



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,347	05/18/2005	Edmond Toy	UN02 0458.US	7132

24738 7590 02/13/2008
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
370 W. TRIMBLE ROAD MS 91/MG
SAN JOSE, CA 95131

EXAMINER

NEFF, MICHAEL R

ART UNIT	PAPER NUMBER
----------	--------------

2611

MAIL DATE	DELIVERY MODE
-----------	---------------

02/13/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/535,347

Applicant(s)

TOY ET AL.

Examiner

Michael R. Neff

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,7-11 and 17-21 is/are rejected.
- 7) ☒ Claim(s) 3-6, 12-16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 1, 2 and 7-11 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-6 of prior U.S. Patent No. 7,138,821 B2. This is a double patenting rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 8, 9, 12, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshino (US Patent 3,601,811) in view of Lee et al. (herein after Lee) (US Patent 5,060,067).

Re Claims 1, 8, 9, 12, 17 and 20, Lee discloses a circuit and associated method comprising: a pulse generator (5, 32) capable of generating a masking pulse timed and of sufficient duration to block at a device a reflection signal within a received signal from a transmission line (Co. 2 lines 54-64; Claim 2); and logic for combining the masking pulse with the received signal (Figure 4a), Yoshino further discloses wherein the generated pulse signal is used for error corrections (Claim 2), but fails to explicitly disclose wherein the interference signal is substantially blocked at a blocking filter; and wherein the device is a receiver device which is connected closer to an input end of the transmission line than an output end of the transmission line as recited in claims 8 and 20; and wherein the blocking filter comprises a digital filter circuit disposed at an input of the device as recited in claim 9.

This design for removing reflected interference is however disclosed by Lee. Lee discloses a system where the interference signal is substantially blocked at a blocking filter (120; Col. 1 lines 10-31) and wherein the device is a receiver device which is connected closer to an input end of the transmission line than an output end of the transmission line (Figure 1, 120) and wherein the blocking filter comprises a digital filter circuit disposed at an input of the device (Figure 1, 120).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the generated signal driving filter characteristics to remove the interference from the received signal as disclosed by Lee with the design of dynamically generating pulses to be incorporated into a received signal in order to correct interference errors or deficiencies in the signal in order to gain the benefit of utilizing a dynamic signal error correction means within the receiver apparatus wherein interference as well as the reflected signal interference can be removed from the received signals.

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshino and Lee and further in view of Kwok (US Patent 5,265,038).

Re Claim 10, Yoshino discloses a network comprising: wherein a reflection signal arises with transmission of a signal across the transmission line; a device connected to the transmission line for receiving the signal, the device comprising: a pulse generator for generating a masking pulse timed and of sufficient duration to block the reflection signal, and logic for combining the masking pulse with the signal received from the transmission line, wherein the reflection signal is blocked by the masking pulse.

However Yoshino fails to explicitly disclose wherein (1) the network comprises a bus system having a transmission line, and further (2) wherein the device is including a blocking filter and wherein the device is connected closer to an input end of the transmission line than an output end of the transmission line, and wherein the blocking

filter comprises a digital filter circuit disposed at an input of the device as recited in claim 11.

Regarding item (1) above, Kwok discloses a pulse filter uses means of pulse interference correction wherein the network comprises a bus system having a transmission line (Figure 1 and 2a).

Therefore it would have been obvious one of ordinary skill in the art at the time the invention was made to incorporate the bus device design as disclosed by Kwok with the system design of Yoshino in order to gain the benefit of incorporating the interference cancelling means into a bus peripheral device.

Regarding item (2) above this design for removing reflected interference is however disclosed by Lee. Lee discloses a system device wherein the device is including a blocking filter and further where the interference signal is substantially blocked at a blocking filter (120; Col. 1 lines 10-31); and wherein the blocking filter comprises a digital filter circuit disposed at an input of the device (Figure 1, 120).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the generated signal driving filter characteristics to remove the interference from the received signal as disclosed by Lee with the design of dynamically generating pulses to be incorporated into a received signal in order to correct interference errors or deficiencies in the signal in order to gain the benefit of utilizing a dynamic signal error correction means within the receiver apparatus wherein interference as well as the reflected signal interference can be removed from the received signals.

7. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshino and Lee as applied to claims 1 and 17 above, and further in view of Kwok.

Re Claims 7 and 18, the combined disclosures of Yoshino and Lee as a whole disclose the circuit of claims 1 and 17, but fail to explicitly disclose wherein the transmission line has mismatched impedance termination at an output end thereof; or the method further comprising lengthening the masking pulse prior to combining thereof with the received signal to insure that the masking pulse completely blocks the reflection signal, said lengthening being accomplished in part by using the received signal as recited in claim 18. This design aspect is however disclosed by Kwok.

Kwok discloses a bus interface wherein the transmission line has mismatched impedance termination at an output end thereof (Col. 2 lines 15-17); and the method further comprising lengthening the masking pulse prior to combining thereof with the received signal to insure that the masking pulse completely blocks the reflection signal, said lengthening being accomplished in part by using the received signal (Figure 4, element 4e).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosure of Kwok as teaching about possible error source within a communication network with the combined disclosures of Yoshino and Lee in order to gain the benefit of having a more dynamic and

comprehensive application of the disclosed signal interference correction system given the application to bus peripheral devices.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshino and Lee as applied to claim 17 above, and further in view of Teymouri (US Patent 5,112,098).

Re Claim 19, the combined teachings of Yoshino and Lee as a whole disclose the method of claim 17, however they fail to explicitly disclose wherein the method further comprising generating the masking pulse on either a falling edge or a rising edge of a state change in the received signal, wherein a reflection signal on either the falling edge or the rising edge is substantially blocked by the masking pulse.

This method is however disclosed by Teymouri. Teymouri discloses a glitch removing system wherein both the rising and falling edges of a signal pulse of adjusted for interference glitches (Abstract; Col. 4 lines 31-40).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of analyzing both the rising and falling edge of signal pulses with the disclosure of the interference removing method as disclosed by Yoshino and Lee in order to gain the benefit of fully analyzing the signal and generating and even more clearly disclosed removed signal through the system.

Allowable Subject Matter

9. Claims 3-5 and 12-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to anticipate or render obvious the disclosure wherein the delay circuit wherein the inverted output logic drives at least one memory gate which drives a reset input a memory of which the output is inverted to provide an inverted masking pulse.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R. Neff whose telephone number is (571) 270-1848. The examiner can normally be reached on Monday - Friday 8:00am - 4:30pm EST ALT Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571)272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/535,347
Art Unit: 2611

Page 9

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael R. Neff
Examiner
Art Unit 2611
(571) 270-1848
Michael.Neff@uspto.gov



SHUWANG LIU
SUPERVISORY PATENT EXAMINER